Chapter 11
Operational Amplifiers and Applications
Chapter Goals

• Understand the “magic” of negative feedback and the characteristics of ideal op amps.
• Understand the conditions for non-ideal op amp behavior so they can be avoided in circuit design.
• Demonstrate circuit analysis techniques for ideal op amps.
• Characterize inverting, non-inverting, summing and instrumentation amplifiers, voltage follower and first order filters.
• Learn the factors involved in circuit design using op amps.
• Find the gain characteristics of cascaded amplifiers.
• Special Applications: The inverted ladder DAC and successive approximation ADC
Differential Amplifier Model: Basic

Represented by:

\[ A = \text{open-circuit voltage gain} \]

\[ v_{id} = (v^+ - v^-) = \text{differential input signal voltage} \]

\[ R_{id} = \text{amplifier input resistance} \]

\[ R_o = \text{amplifier output resistance} \]

The signal developed at the amplifier output is in phase with the voltage applied at the + input (non-inverting) terminal and \(180^\circ\) out of phase with that applied at the - input (inverting) terminal.
LM741 Operational Amplifier: Circuit Architecture

Schematic Diagram

Current Mirrors

[Diagram of LM741 Operational Amplifier]
Ideal Operational Amplifier

- The “ideal” op amp is a special case of the ideal differential amplifier with infinite gain, infinite $R_{id}$ and zero $R_o$.

\[ v_{id} = \frac{v_o}{A} \quad \text{and} \quad \lim_{A \to \infty} v_{id} = 0 \]

- If $A$ is infinite, $v_{id}$ is zero for any finite output voltage.
- Infinite input resistance $R_{id}$ forces input currents $i_+$ and $i_-$ to be zero.

- The ideal op amp operates with the following assumptions:
  - It has infinite common-mode rejection, power supply rejection, open-loop bandwidth, output voltage range, output current capability and slew rate
  - It also has zero output resistance, input-bias currents, input-offset current, and input-offset voltage.
The Inverting Amplifier: Configuration

- The positive input is grounded.
- A “feedback network” composed of resistors $R_1$ and $R_2$ is connected between the inverting input, signal source and amplifier output node, respectively.
Inverting Amplifier: Voltage Gain

- The negative voltage gain implies that there is a $180^0$ phase shift between both dc and sinusoidal input and output signals.
- The gain magnitude can be greater than 1 if $R_2 > R_1$
- The gain magnitude can be less than 1 if $R_1 > R_2$
- The inverting input of the op amp is at ground potential (although it is not connected directly to ground) and is said to be at virtual ground.

\[ v_s - i_s R_1 - i_2 R_2 - v_o = 0 \]

But \( i_s = i_2 \) and \( v_o = 0 \) (since \( v_{id} = v_+ - v_- = 0 \))

\[ \therefore i_s = \frac{v_s}{R_1} \quad \text{and} \quad A_v = \frac{v_o}{v_s} = -\frac{R_2}{R_1} \]
Inverting Amplifier: Input and Output Resistances

\( R_{\text{in}} = \frac{v_s}{i_s} = R_1 \) since \( v_- = 0 \)

\( v_x = i_2 R_2 + i_1 R_1 \)

\[ But \ i_1 = i_2 \]

\[ \therefore v_x = i_1 (R_2 + R_1) \]

Since \( v_- = 0, \ i_1 = 0 \). Therefore \( v_x = 0 \) irrespective of the value of \( i_x \).

\[ \therefore R_{\text{out}} = 0 \]

\( R_{\text{out}} \) is found by applying a test current (or voltage) source to the amplifier output and determining the voltage (or current) after turning off all independent sources. Hence, \( v_s = 0 \).
Inverting Amplifier: Example

- **Problem:** Design an inverting amplifier
- **Given Data:** $A_v = 20 \text{ dB}$, $R_{in} = 20k\Omega$,
- **Assumptions:** Ideal op amp
- **Analysis:** Input resistance is controlled by $R_1$ and voltage gain is set by $R_2 / R_1$.

\[ A_v(dB) = 20 \log_{10} \left( |A_v| \right), \quad \therefore |A_v| = 10^{40 \text{dB}/20\text{dB}} = 100 \quad \text{and} \quad A_v = -100 \]

A minus sign is added since the amplifier is inverting.

\[ R_1 = R_{in} = 20k\Omega \]
\[ A_v = -\frac{R_2}{R_1} \Rightarrow R_2 = 100R_1 = 2M\Omega \]
The Non-inverting Amplifier: Configuration

- The input signal is applied to the non-inverting input terminal.
- A portion of the output signal is fed back to the negative input terminal.
- Analysis is done by relating the voltage at $v_1$ to input voltage $v_s$ and output voltage $v_o$. 
Non-inverting Amplifier: Voltage Gain, Input Resistance and Output Resistance

Since $i_- = 0$  
\[ v_1 = v_o \frac{R_1}{R_1 + R_2} \]  
and  
\[ v_s - v_{id} = v_1 \]

But $v_{id} = 0$  
\[ \therefore v_s = v_1 \]

\[ v_o = v_s \frac{R_1 + R_2}{R_1} \]

\[ \therefore A_v = \frac{v_o}{v_s} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \]

Since $i_+ = 0$  
\[ R_{in} = \frac{v_s}{i_+} = \infty \]

$R_{out}$ is found by applying a test current source to the amplifier output after setting $v_s = 0$. It is identical to the output resistance of the inverting amplifier i.e. $R_{out} = 0$. 
Non-inverting Amplifier: Example

- **Problem:** Determine the output voltage and current for the given non-inverting amplifier.

- **Given Data:** \( R_1 = 3k\Omega, \ R_2 = 43k\Omega, \ v_s = +0.1 \text{ V} \)

- **Assumptions:** Ideal op amp

- **Analysis:**

  \[
  A_v = 1 + \frac{R_2}{R_1} = 1 + \frac{43k\Omega}{3k\Omega} = 15.3
  \]

  \[
  v_o = A_v v_s = (15.3)(0.1\text{V}) = 1.53\text{V}
  \]

  Since \( i_\text{in} = 0 \),

  \[
  i_o = \frac{v_o}{R_2 + R_1} = \frac{1.53\text{V}}{43k\Omega + 3k\Omega} = 33.3\mu\text{A}
  \]
Finite Open-loop Gain and Gain Error

The feedback factor, $\beta$, is called the feedback factor. $v_1 = \frac{R_1}{R_1 + R_2} v_o = \beta v_o$

$\beta = \frac{R}{R_1 + R_2}$ is called the feedback factor.

$v_o = A v_{id} = A(v_s - v_1) = A(v_s - \beta v_o)$

$A_v = \frac{v_o}{v_s} = \frac{A}{1 + A\beta}$

$A\beta$ is called loop gain.

For $A\beta \gg 1$,

$A_v \approx \frac{1}{\beta} = 1 + \frac{R_2}{R_1}$

This is the “ideal” voltage gain of the amplifier. If $A\beta$ is not $\gg 1$, there will be “Gain Error”.

If $\gamma = i = 1$, $i = \frac{R_2}{R_1}$
Gain Error

- Gain Error is given by
  \[ GE = (\text{ideal gain}) - (\text{actual gain}) \]
  For the non-inverting amplifier,
  \[ GE = \frac{1}{\beta} - \frac{A}{1 + A\beta} = \frac{1}{\beta(1 + A\beta)} \]
- Gain error is also expressed as a fractional or percentage error.
  \[ FGE = \frac{1}{\beta} - \frac{A}{1 + A\beta} = \frac{1}{1 + A\beta} \approx \frac{1}{A\beta} \]
  \[ PGE \approx \frac{1}{A\beta} \times 100\% \]
Gain Error: Example

- **Problem**: Find ideal and actual gain and gain error in percent
- **Given data**: Closed-loop gain of 100,000, open-loop gain of 1,000,000.
- **Approach**: The amplifier is designed to give ideal gain and deviations from the ideal case have to be determined. Hence, \( \beta = \frac{1}{10^5} \).

*Note: \( R_1 \) and \( R_2 \) aren’t designed to compensate for the finite open-loop gain of the amplifier.*

- **Analysis**:
  \[
  A_v = \frac{A}{1 + A\beta} = \frac{10^6}{1 + \frac{10^6}{10^5}} = 9.09 \times 10^4
  \]
  \[
  \text{PGE} = \frac{10^5 - 9.09 \times 10^4}{10^5} \times 100\% = 9.09\%
  \]
Output Voltage and Current Limits

Practical op amps have limited output voltage and current ranges.

Voltage: Usually limited to a few volts less than power supply span.

Current: Limited by additional circuits (to limit power dissipation or protect against accidental short circuits).

The current limit is frequently specified in terms of the minimum load resistance that the amplifier can drive with a given output voltage swing. Eg: \[ |i_o| = \frac{5V}{500\Omega} = 10\text{mA} \]

\[ i_o = i_L + i_F = \frac{V_o}{R_L} + \frac{V_o}{R_2 + R_1} = \frac{V_o}{R_{EQ}} \]

\[ R_{EQ} = R_L \left| R_1 + R_2 \right| \]

For the inverting amplifier,

\[ R_{EQ} = R_L \left| R_2 \right| \]
Example PSpice Simulations of Non-inverting Amplifier Circuits
Non-inverting Amplifier
Ideal Gain 1001

Frequency: 100Hz
Amplitude: 5mV

R1: 100Ω
R2: 100kΩ

V1 DC = 9
V2 DC = 9
Non-inverting Amplifier

Ideal Gain 1001 with
500 ohm load

V_i
AMPLITUDE = 5m
FREQUENCY = 100

uA741

V_o

DC = 9

R1
100

R2
100k

RL
500

V1

V2

5.8V

0V

-5.8V

Time

v(t) = v(t)
Non-inverting Amplifier
Ideal Gain 1001 with 100 ohm load

AMPLITUDE = 5m
FREQUENCY = 100

V1 DC = 9
V2 DC = 9

R1 100
R2 100
100k

0
The Unity-gain Amplifier or “Buffer”

- This is a special case of the non-inverting amplifier, which is also called a voltage follower, with infinite $R_1$ and zero $R_2$. Hence $A_v = 1$.
- It provides an excellent impedance-level transformation while maintaining the signal voltage level.
- The “ideal” buffer does not require any input current and can drive any desired load resistance without loss of signal voltage.
- Such a buffer is used in many sensor and data acquisition system applications.
The Summing Amplifier

Since the negative amplifier input is at virtual ground,

\[ i_1 = \frac{v_1}{R_1} \quad i_2 = \frac{v_2}{R_2} \quad i_3 = -\frac{v_o}{R_3} \]

Since \( i_3 = 0 \), \( i_3 = i_1 + i_2 \),

\[ \therefore v_o = -\frac{R_3}{R_1} v_1 - \frac{R_3}{R_2} v_2 \]

- Scale factors for the 2 inputs can be independently adjusted by the proper choice of \( R_2 \) and \( R_1 \).
- Any number of inputs can be connected to a summing junction through extra resistors.
- This circuit can be used as a simple digital-to-analog converter. This will be illustrated in more detail, later.
The Difference Amplifier

The circuit is also called a differential amplifier, since it amplifies the difference between the input signals.

For \( v_2 = 0 \), the circuit reduces to an inverting amplifier.

For general case, \( i_1 \) is a function of both \( v_1 \) and \( v_2 \).

Since \( v_-= v_+ \),
\[
 v_o = -\frac{R_2}{R_1} (v_1 - v_2)
\]

For \( R_2 = R_1 \),
\[
 v_o = -(v_1 - v_2)
\]

- This circuit is also called a differential amplifier, since it amplifies the difference between the input signals.
- \( R_{in2} \) is series combination of \( R_1 \) and \( R_2 \) because \( i_+ \) is zero.
- For \( v_2 = 0 \), \( R_{in1} = R_1 \), as the circuit reduces to an inverting amplifier.

Also,
\[
 v_+ = \frac{R_2}{R_1 + R_2} v_2
\]
Difference Amplifier: Example

- **Problem:** Determine \( v_o \)
- **Given Data:** \( R_1 = 10k\Omega, \) \( R_2 = 100k\Omega, \) \( v_1 = 5 \) V, \( v_2 = 3 \) V
- **Assumptions:** Ideal op amp. Hence, \( v_- = v_+ \) and \( i_- = i_+ = 0. \)
- **Analysis:** Using dc values,

\[
A_{dm} = -\frac{R_2}{R_1} = -\frac{100k\Omega}{10k\Omega} = -10
\]

\[
V_o = A_{dm} (V_1 - V_2) = -10(5 - 3)
\]

\[
V_o = -20.0 \text{ V}
\]

Here \( A_{dm} \) is called the “differential mode voltage gain” of the difference amplifier.
Finite Common-Mode Rejection Ratio (CMRR)

A real amplifier responds to signal common to both inputs, called the common-mode input voltage ($v_{ic}$). In general,

$$v_o = A_{dm}(v_1 - v_2) + A_{cm} \left( \frac{v_1 + v_2}{2} \right)$$

$$v_o = A_{dm}(v_{id}) + A_{cm}(v_{ic})$$

$A$(or $A_{dm}$) = differential-mode gain
$A_{cm}$ = common-mode gain
$v_{id}$ = differential-mode input voltage
$v_{ic}$ = common-mode input voltage

$$v_1 = v_{ic} + \frac{v_{id}}{2} \quad v_2 = v_{ic} - \frac{v_{id}}{2}$$

An ideal amplifier has $A_{cm} = 0$, but for a real amplifier,

$$v_o = A_{dm} \left( v_{id} + \frac{A_{cm} v_{ic}}{A_{dm}} \right) = A_{dm} \left( v_{id} + \frac{v_{ic}}{CMRR} \right)$$

$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right|$

and $CMRR(\text{dB}) = 20 \log_{10}(CMRR)$
Finite Common-Mode Rejection Ratio: Example

- **Problem:** Find output voltage error introduced by finite CMRR.
- **Given Data:** $A_{dm} = 2500$, CMRR = 80 dB, $v_1 = 5.001$ V, $v_2 = 4.999$ V
- **Assumptions:** Op amp is ideal, except for CMRR. Here, a CMRR in dB of 80 dB corresponds to a CMRR of $10^4$.
- **Analysis:**
  
  - $v_{id} = 5.001$ V - 4.999 V
  - $v_{ic} = \frac{5.001$ V + 4.999 V}{2} = 5.000$ V
  - $v_o = A_{dm} \left( v_{id} + \frac{v_{ic}}{\text{CMRR}} \right) = 2500 \left( 0.002 + \frac{5.000}{10^4} \right) V = 6.25$ V

  In the "ideal" case, $v_o = A_{dm} v_{id} = 5.00$ V

  % output error = \frac{6.25 - 5.00}{5.00} \times 100\% = 25\%$

  The output error introduced by finite CMRR is 25% of the expected ideal output.
uA741 CMRR Test: Differential Gain

Difference Amplifier -- Differential Gain Test
Differential Gain $A_{dm} = \frac{5 \text{ V}}{5 \text{ mV}} = 1000$
uA741 CMRR Test: Common Mode Gain

Difference Amplifier -- Common Mode Gain Test
Common Mode Gain $A_{cm} = 160 \text{ mV}/5 \text{ V} = .032$
CMRR Calculation for uA741

\[
\text{CMRR} = \frac{|A_{\text{dm}}|}{|A_{\text{cm}}|} = \frac{1000}{0.032} = 3.125 \times 10^4
\]

\[
\text{CMRR (dB)} = 20 \log_{10} (\text{CMRR}) = 89.9 \text{ dB}
\]
Instrumentation Amplifier

Combines 2 non-inverting amplifiers with the difference amplifier to provide higher gain and higher input resistance.

Ideal input resistance is infinite because input current to both op amps is zero. The CMRR is determined only by Op Amp 3.

\[
\begin{align*}
v_o &= -\frac{R}{4} (v_a - v_b) \\
v_a - iR_2 - i(2R_1) - iR_2 &= v_b \\
i &= \frac{v - v}{2R_1} \\
\therefore v_o &= -\frac{R}{4} \left(1 + \frac{R_2}{R_1}\right) (v_1 - v_2)
\end{align*}
\]
Instrumentation Amplifier: Example

- **Problem**: Determine $V_o$

- **Given Data**: $R_1 = 15 \, \text{k}\Omega$, $R_2 = 150 \, \text{k}\Omega$, $R_3 = 15 \, \text{k}\Omega$, $R_4 = 30 \, \text{k}\Omega$, $V_1 = 2.5 \, \text{V}$, $V_2 = 2.25 \, \text{V}$

- **Assumptions**: Ideal op amp. Hence, $v_- = v_+$ and $i_- = i_+ = 0$.

- **Analysis**: Using dc values,

$$A_{dm} = -\frac{R_4}{R_3} \left( 1 + \frac{R_2}{R_1} \right) = -\frac{30\,\text{k}\Omega}{15\,\text{k}\Omega} \left( 1 + \frac{150\,\text{k}\Omega}{15\,\text{k}\Omega} \right) = -22$$

$$V_o = A_{dm} (V_1 - V_2) = -22 (2.5 - 2.25) = -5.50 \, \text{V}$$
The Active Low-pass Filter

Use a phasor approach to gain analysis of this inverting amplifier. Let \( s = j \omega \).

\[
A_v = \frac{\tilde{v}_o(j\omega)}{\tilde{v}(j\omega)} = \frac{Z_2(j\omega)}{Z_1(j\omega)} \quad Z_1(j\omega) = R_1
\]

\[
Z_2(j\omega) = \frac{1}{sC} \frac{R_2}{R_2 + \frac{1}{j\omega C}} = \frac{R_2}{j\omega CR_2 + 1}
\]

\[
A_v = -\frac{R_2}{R_1} \frac{1}{1 + j\omega CR_2} = \frac{R_2}{R_1} e^{j\pi} \frac{1}{1 + \frac{j\omega}{\omega_c}}
\]

\[
\omega_c = 2\pi f_c = \frac{1}{R_2 C} \quad \therefore f_c = \frac{1}{2\pi R_2 C}
\]

\( f_c \) is called the high frequency “cutoff” of the low-pass filter.
Active Low-pass Filter (continued)

- At frequencies below \( f_c \) (\( f_H \) in the figure), the amplifier is an inverting amplifier with gain set by the ratio of resistors \( R_2 \) and \( R_1 \).

- At frequencies above \( f_c \), the amplifier response “rolls off” at -20dB/decade.

- Notice that cutoff frequency and gain can be independently set.

\[
A_v = \frac{R_2}{R_1} \left[ e^{j\pi} \frac{1}{1 + \frac{j\omega}{\omega_c}} \right] = \frac{R_2}{R_1} \left[ e^{j\pi} \frac{1}{1 + \frac{j\tan^{-1}(\omega/\omega_c)}{2}} \right] = \frac{R_2}{R_1} e^{j[\pi - \tan^{-1}(\omega/\omega_c)]}
\]

magnitude  phase
Active Low-pass Filter: Example

- **Problem:** Design an active low-pass filter
- **Given Data:** $A_v = 40 \text{ dB}, R_{in} = 5 \text{ k}\Omega, f_H = 2 \text{ kHz}$
- **Assumptions:** Ideal op amp, specified gain represents the desired low-frequency gain.
- **Analysis:**
  \[
  |A_v| = 10^{40/20} = 100
  \]
  Input resistance is controlled by $R_1$ and voltage gain is set by $R_2 / R_1$. The cutoff frequency is then set by $C$.

  \[
  R_1 = R_{in} = 5 \text{ k}\Omega \quad \text{and} \quad |A_v| = \frac{2}{R_1} \implies R_2 = 100R_1 = 500 \text{ k}\Omega
  \]

  \[
  C = \frac{1}{2\pi f_H R_2} = \frac{1}{2\pi(2\text{ kHz})(500 \text{ k}\Omega)} = 159 \text{ pF}
  \]

  The closest standard capacitor value of 160 pF lowers cutoff frequency to 1.99 kHz.
Low-pass Filter Example PSpice Simulation

Low-pass Filter Example
Pass-band Gain = 100
Cutoff Frequency = 2 kHz
Output Voltage Amplitude in dB
Output Voltage Amplitude in Volts (V) and Phase in Degrees (d)
Cascaded Amplifiers

- Connecting several amplifiers in cascade (output of one stage connected to the input of the next) can meet design specifications not met by a single amplifier.
- Each amplifier stage is built using an op amp with parameters $A$, $R_{id}$, $R_o$, called open loop parameters, that describe the op amp with no external elements.
- $A_v$, $R_{in}$, $R_{out}$ are closed loop parameters that can be used to describe each closed-loop op amp stage with its feedback network, as well as the overall composite (cascaded) amplifier.
Two-port Model for a 3-stage Cascade Amplifier

- Each amplifier in the 3-stage cascaded amplifier is replaced by its 2-port model.

\[
V_o = A_{vA} V_s \left( \frac{R_{inB}}{R_{outA} + R_{inB}} \right) A_{vB} \left( \frac{R_{inC}}{R_{outB} + R_{inC}} \right) A_{vC}
\]

Since \( R_{out} = 0 \),

\[
A_v = \frac{V_o}{V_s} = A_{vA} A_{vB} A_{vC}
\]

\( R_{in} = R_{inA} \) and \( R_{out} = R_{outC} = 0 \).
A Problem: Voltage Follower Closed Loop Gain Error due to $A$ and CMRR

The ideal gain for the voltage follower is unity. The gain error here is:

$$GE = 1 - A_v = \frac{1}{1 + A} \left( 1 - \frac{1}{2 \text{CMRR}} \right)$$

Since, both $A$ and CMRR are normally $\gg 1$,

$$GE \approx \frac{1}{A} - \frac{1}{\text{CMRR}}$$

Since $A \sim 10^6$ and CMRR $\sim 10^4$ at low to moderate frequency, the gain error is quite small and is, in fact, usually negligible.
Inverted R-2R Ladder DAC

- A very common DAC circuit architecture with good precision.
- Currents in the ladder and the reference source are independent of digital input. This contributes to good conversion precision.
- Complementary currents are available at the output of inverted ladder.
- The “bit switches” need to have very low on-resistance to minimize conversion errors.
Successive Approximation ADC

- Binary search is used by the SAL to determine $v_X$.
- $n$-bit conversion needs $n$ clock periods. Speed is limited by the time taken by the DAC output to settle within a fraction of an LSB of $V_{FS}$, and by the comparator to respond to input signals differing by small amounts.
- Slowly varying input signals, not changing by more than 0.5 LSB ($V_{FS}/2^{n+1}$) during the conversion time ($T_T = nT_C$) are acceptable.
- For a sinusoidal input signal with p-p amplitude = $V_{FS}$, $f_o \leq \frac{f_c}{2^{n+2}(n+1)\pi}$
- To avoid this frequency limitation, a high speed sample-and-hold circuit is used ahead of the successive approximation ADC.
- This is a very popular ADC with fast conversion times, used in 8- to 16-bit converters.
SAADC: Block Diagram

**Figure 4.8** Successive-approximation converter with a sample-and-hold device
SAADC: Method of Operation

Figure 4.7 Successive-approximation method for analog-to-digital conversion.